

# Strained Silicon NMOS Devices With Embedded Source/Drain

## Abstract

A planar NFET on a strained silicon layer supported by a SiGe layer achieves reduced external resistance by removing SiGe material outside the transistor body and below the strained silicon layer and replacing the removed material with epitaxial silicon, thereby providing lower resistance for the transistor electrodes and permitting better control over Arsenic diffusion.